In Section 3 of the Office Action, the Examiner objected to the drawings because they included reference characters not mentioned in the description.

In regard to ref. char. 34, Applicants are submitting a proposed drawing correction for Fig. 1 deleting the ref. char. 34. Approval of this drawing correction is respectfully requested.

In regard to ref. char. 26, the Examiner is requested to view page 5, line 18.

In regard to ref. chars. 90 and 92, the Examiner is requested to view page 5, line 20.

In regard to ref. char. 132, Applicants are submitting a proposed drawing correction for Fig. 2 deleting the ref. char. 132. Approval of this drawing correction is respectfully requested.

In regard to ref. char. 317, Applicants have amended the specification with the paragraph starting on page 10 line 7 to include the appropriate labeling for block 317 to make the specification consonant with the drawings. Also, the Applicants are submitting a proposed drawing correction for Fig. 7 to correct a typographical error in block 317 changing "contracts" to "contacts." Approval of this drawing correction is respectfully requested.

In regard to ref. char. 258, Applicants are submitting a proposed drawing correction for Fig. 10 deleting the ref. char. 258. Approval of this drawing correction is respectfully requested.

In Section 4 of the Office Action, the Examiner objected to the drawings because a) reference character 127 had been used to designate both bulk and substrate body; b) ref. char. 13 has been used to designate both address and diode; and c) ref. char. 46 has been used to designate both primitive driveline and primitive signal interface.

In regard to ref. char. 127, the Applicants have amended the specification in the paragraph beginning on page 9, line 15 to remove the ref. char. 127 with respect to the "bulk."

In regard to ref. char. 13, the Applicants are submitting a proposed drawing correction to Fig. 6 deleting the ref. char. 13 for the address. Approval of this drawing correction is respectfully requested.

In regard to ref. char. 46, the Applicants have amended the specification to change the "signal interface" to "driveline" in the paragraph beginning on page 9, line 15.

In Section 5 of the Office Action, the Examiner objected to claims 8-10 and 18-20 because the way the preamble was written, it was not clear whether the claim is independent or dependent. Applicants respectfully traverse the objection and note that this dependent form of claiming is permissible as held by the Board of Patent Appeals and Interferences in in re Moelands, 3 USPQ.2D 1474 (1987).

Applicants assert that claims 8-10 and 18-20 are proper *dependent* claims that comply with 35 USC 112, 4th paragraph. Each constitute "a further limitation of the subject matter claimed," are not broader than their parent claims. In addition, no element of any respective parent claim is deleted or replaced by any other element in claims 8-10 and 18-20. These claims incorporate by reference all the limitations of the claim to which each refers as required by 35 USC 112, 4th paragraph. Furthermore, a product which would infringe a printhead of claims 8 and 18, a fluid cartridge of claims 9 and 19, and a recording device of claims 10 and 20, would also infringe the respective parent claim. The Board in in re Moelands noted that they read MPEP §608.01(n) (Dec. 1985) as being consistent with their decision. Accordingly, the Applicants have chosen to not change the wording of claims 8-10 and 18-20 as requested by the Examiner.

In Section 7 of the Office Action, the Examiner rejected claims 5, 9, 10, and 18-20 under 35 USC 112, 2nd paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. In particular, the Examiner stated that it is unclear what is meant by bulk in claim 5 and fluidically in claims 9, 18, and 19.

"Bulk" is a term of art in integrated circuit technology that means the "well" or "substrate" if there is no well in which the transistor resides. The "bulk is typically semiconductor material of opposite polarity of the source and drain material. By biasing the "bulk," the voltage-current characteristics of the transistor can be modified. Applicants on page 7, line 8 equate the "bulk" to the "backgates or bodies of the transistors formed in the substrate." On page 9, lines 15-19 of the Application, the Applicants state "that the bulk of transistor 130 is shown as having an inherent diode 13 between the bulk and source connections." This is due to the transistor structure not having a substrate contact to the source as is conventionally done in MOS circuits. In an accompanying IDS, a copy of portions of a textbook (Grob) in basic electronics describes the "bulk" as the substrate and its appropriate symbolic representation as used in electronic symbols. The Applicants have not used the term "bulk" in any other manner than that known and used as one skilled in the art. Accordingly, Applicants respectfully request removal of the rejection of claim 5 under 35 USC 112, 2nd paragraph.

"Fluidically" is an adverb form of "fluidic" and is commonly used as a term of art in indicating that the connection between two components is "fluidic." Several patents use this term, see for instance US 5,103,246. Also, a search on Google under "fluidically coupled" shows the term is widely used and its meaning well understood by those of skill in the art. Accordingly, Applicants respectfully request removal of the rejection of claims 9, 18, and 19 under 35 USC 112, 2nd paragraph.

In Section 9 of the Office Action, the Examiner rejected claims 1, 2, 6-9, 11, 12, 16-19, 21-24, 27, and 28 under 35 USC 103(a) as being obvious over Hess et al. (5,122,812). Applicants respectfully traverse this rejection for the reasons stated herein.

In particular for claims 1 and 11, Hess does not describe "an ejection element coupled to the transistor wherein the ejection element is disposed over the substrate without an intervening field oxide layer" as the Examiner suggests

Hess indicates in its Fig. 11. Fig. 11 clearly shows the upper layer 72 which is formed by thermal oxidation or by heating the lower portion 71 of substrate 70 until a desired layer of silicon dioxide has been formed (see col. 5, lines 1-18). Hess describes what is known in the art as a field oxide (FOX) layer. In addition, the Examiner agrees that Hess does not disclose that the gate forms a closed loop but that asserts that "it is well known that gates form loops." However, while a gate may be formed in a loop, not all gates have formed loops. By having the all the gates on an integrated circuit formed by loops and eliminating the field oxide layer and thus the need to have a island mask, a simpler structure is formed to is more cost efficient and more reliable over the structure shown in Hess. In view of that, Applicants have amended claim 1 to more clearly define and distinguish their invention over the art made of record. Claim 1, as amended, now clearly states that the integrated circuit has a set of transistors wherein the gates of each of the set of transistors forms at least one closed loop. It is Applicants' claimed combination, as amended, and invention as a whole which is not disclosed, taught, or suggested by the art made of record. Claim 11 already includes the limitations of "a set of transistors, wherein all transistors on the substrate are formed with at least one closed loop structure" and the "set of ejection elements" are "disposed over the substrate without an intervening field oxide layer." Accordingly, removal of the rejection under 35 USC 103(a) for claims 1 and 11 is respectfully requested.

Claims 5, 6, and 7 have been amended to correct antecedent issues arising from the amendment of claim 1.

In regard to claims 2 and 12, the Examiner states that Hess discloses a dielectric layer disposed between the ejection element and the substrate having a thickness greater than 2000 Angstroms. However, as discussed for claim 1, Hess discloses a FOX dielectric layer. Applicants instead are claiming not a FOX dielectric layer but a non-FOX dielectric layer ("without an intervening field oxide layer"). One advantage of Applicants non-FOX dielectric layer is that the contact etch process is shortened (see page 6, lines 12-20). Further, the non-FOX dielectric layer is deposited after the transistor is formed thus allowing for the

elimination of an island mask and several steps in a conventional process. This helps to reduce the cost of the claimed invention. Accordingly Hess does not disclose, teach, or suggest Applicants' claimed invention. Removal of the rejection under 35 USC 103(a) for claims 2 and 12 is respectfully requested.

In regard to claims 6 and 16, the Examiner states that the limitation "the transistor is formed without an active mask definition" makes it a product by process claim. The Examiner states that the Applicant has the burden of proof that the product is structurally different. As stated above, Hess does not disclose a printhead that does not have a field oxide layer. Nor does Hess disclose a set of transistors that each has at least one closed loop as Applicants are claiming. Applicants claimed structure in combination is not disclosed, taught, or suggested by Hess and results in a different structure than that shown in Hess although the two structures perform similar operations. Accordingly, removal of the rejection under 35 USC 103(a) for claims 6 and 16 is respectfully requested.

In regard to claims 7, 17, 8, 18, 9, and 19, these dependent claims depend directly or indirectly on claims 1 and 11 and are believed at least patentable based on the patentability of their respective parent claims.

In regard to claim 21, the Applicants have amended claim 21 to more clearly define and distinguish their invention over the art made of record. Now claim 21 as amended has a layer of silicon dioxide that is not field oxide grown and each of the set of transistors has a closed loop structure. It is these elements in combination that are not disclosed, taught or suggested by the art made of record as discussed above for claims 1 and 11. Removal of the rejection under 35 USC 103(a) for claim 21 is respectfully requested.

In regard to claims 22-28, these dependent claims depend directly on claim 21 and are believed at least patentable based on the patentability of claim 21. Removal of the rejection under 35 USC 103(a) for claims 22 –28 is respectfully requested.

In Section 10 of the Office Action, the Examiner rejected claims 3, 13, and 25 under 35 USC 103(a) as being obvious over Hess (5,122,812, hereafter

Hess'812) in view of Hess (4,719,477, hereafter Hess'477). Applicants respectfully traverse the rejection. Dependent claims 3, 13, and 25 depend on independent claims 1, 11, and 21 and are believe at least patentable based on the patentability of their respective parent claims. Further, these claims are believed separately patentable. Hess'477 describes placing the phosphosilicate glass after the resistor is formed and is used as a protective layer to inhibit the formation of phosphoric acid, however the FOX oxide in Hess'812 is used to isolate the transistors and to provide thermal isolation from the resistor to the substrate. In fact, the FOX of Hess'812 is located between the resistor and the substrate while the phosphosilicate glass of Hess'477 is located between the resistor and the passivation layers and is used to allow the building of the resistor, conductor and passivation layers after the resistor logic and drive transistors have been fabricated. Thus there is no motivation to change the FOX layer with the phosphosilicate layer. Removal of the rejection under 35 USC 103(a) for claims 3, 13, and 25 is respectfully requested.

In Section 11 of the Office Action, the Examiner rejected claims 4, 14, and 26 under 35 USC 103(a) as being obvious over Hess'812 in view of Hawkins. Claims 4, 14, and 26 are believed at least patentable based on the patentability of their respective parent claims 1, 11, and 21. Again, like Hess 477, the thermal oxide-phosphosilicate glass layer of Hawkins is formed on top of the heating element and is not used for thermal isolation to the substrate. Therefore, there is no motivation to substitute the FOX layer of Hess'812 with the overglass layer 13 of Hawkins. Removal of the rejection under 35 USC 103(a) for claims 4, 14, and 26 is respectfully requested.

In Section 12 of the Office Action, the Examiner rejected claims 10 and 20 under 35 USC 103(a) as being obvious over Hess in view of Burke. Dependent claims 10 and 20 are believed at least patentable based on the patentability of their respective parent claims. Removal of the rejection under 35 USC 103(a) is respectfully requested.

The prior art made of record but not relied upon by the Examiner has been reviewed, but is no more pertinent to Applicants' invention than the cited references for the reasons given above.

Applicants believe their claims as amended are patentable over the art of record, and that the amendments made herein are within the scope of a search properly conducted under the provisions of MPEP 904.02. Accordingly, claims 1-28 are deemed to be in condition for allowance, and such allowance is respectfully requested.

Respectfully Submitted,
Frank Bryant et al.
By: Timothy F Myers
Timothy Myers
Patent Attorney
Registration No.
42,919

Hewlett-Packard Company
Legal Department
1000 NE Circle Blvd.
Corvallis, OR 97330
Telephone: (541)715-4197
Fax: (541)715-8581

Appendix A
Clean Copy of Changes

Please replace the paragraph starting on page 4, line 30 with the following:

Fig. 1 is an exemplary cross-section of a conventional integrated circuit 11 that combines a transistor and ejection element. A substrate 10, preferably silicon though other substrates known to those skilled in the art can be used and still meet the spirit and scope of the invention, is processed using conventional integrated circuit processes. The substrate 10 is preferably doped with a p- dopant for an NMOS process; however, it can also be doped with an n- dopant for a PMOS process. The substrate 10 has an ejection element 20 disposed over the substrate with an intervening field oxide layer 12 providing thermal isolation of the ejection element 20 to the substrate 10. Optionally, additional deposited oxide layers may be disposed on the field oxide layer 12. The ejection element 20 is coupled to a transistor 30, preferably an N-MOS transistor, formed in the substrate 10. The coupling is preferably done using a conductive layer 21, such as aluminum, although other conductors can be used such as copper and gold, to name a couple. The transistor 30 includes a source active region 18 and a drain active region 16 and a gate 14. The ejection element 20 is made from a resistive conductive layer 19 that is deposited on the field oxide layer 12. The area of an opening in the conductive layer 21 defines the ejection element 20. To protect the ejection element 20 from the reactive qualities of fluid to be ejected, such as ink, a passivation layer 22 is disposed over the ejection element 20 and other thin-film layers that have been deposited on the substrate 10. To create a printhead, the integrated circuit 11 is combined with an orifice layer 82, shown as a fluid barrier 26 and an orifice plate 28. The ejection element 20 and the passivation layer 22 are protected from damage due to bubble collapse in fluid chamber 92 after fluid ejection from nozzle 90 by a cavitation layer 24 that is disposed over passivation layer 22. The stacks of thin-film layers 32 that are disposed on substrate 10 are those layers processed on the substrate 10 before

applying the orifice layer 82. Optionally, the orifice layer 82 can be a single or multiple layer(s) of polymer or epoxy material. Several methods for creating the orifice layer are known to those skilled in the art.

Please replace the paragraph starting on page 10, line 7 with the following:

Fig. 7 is an exemplary flow chart of a process used to create an integrated circuit that embodies aspects of the invention. In block 310, the process begins with a doped substrate, preferably a p- doped substrate for N-MOS, and an n-doped substrate for PMOS. In a conventional process, the major steps of defining active areas and growing field oxide would be performed. In the process of the invention, the conventional steps of defining of the active areas with an active mask and field oxide growth are eliminated. In block 312, a first dielectric layer of gate oxide is applied on the doped substrate. Preferably, a layer of silicon dioxide is formed to create the gate oxide. Alternatively, the gate oxide can be formed from several layers such as a layer of silicon nitride and a layer of silicon dioxide. Additionally, several different methods of applying the gate oxide are known to those skilled in the art. In block 314, a first conductive layer is applied, preferably a deposition of polycrystalline silicon (polysilicon), and patterned with the gate mask and wet or dry etched in block 316 in closed-loop structures to form the gate regions from the remaining first conductive layer, the drain of the transistors formed within the closed-loop and the source of the transistors in the area outside of the closed-loop structures. In block 318, a dopant concentration is applied in the areas of the substrate that is not obstructed by the first conductive layer to create the active regions of the transistors. A substantial portion of the substrate surface will be created as active region because no island mask is used. In block 320, a second dielectric layer, preferably phosphosilicate glass (PSG) is applied to a predetermined thickness (at least 2000 but preferably between about 6000 to about 12,000 Angstroms or greater) to provide sufficient thermal isolation between a later formed ejection element and the substrate 110. Preferably, after the PSG is

applied, it is densified. Optionally, before applying the second dielectric layer, a thin layer of thermal oxide can be applied over the source, drain and gate of the transistor, preferably to a thickness of about 50 to 2,000 Angstroms but preferably 1000 Angstroms. In block 322, a first set of contact regions is created in the second dielectric layer using the contact mask to form openings to the first conductive layer and/or the active regions of the transistors. Optionally in block 317, a second etch step is used with the optional substrate contact mask to pattern and etch substrate body contacts. In block 324, a second conductive layer, preferably an electrically resistive layer such as tantalum aluminum, is applied by deposition. Optionally, the second conductive layer is formed of polycrystalline silicon (polysilicon). The second conductive layer is used to create the ejection element. In block 326, a third conductive layer, such as aluminum, is applied, preferably by deposition or sputtering. In block 328 the third conductive layer is patterned with the metal1 mask and etch to form metal traces for interconnections. The third conductive layer is used to connect the active regions of the transistors to the ejection elements. The third conductive layer is also used to connect various signals from the first conductive layer to active area regions. To convert the integrated circuit to a printhead further steps combine printhead thin-film protective materials and a conductive layer to interface with the integrated circuit thin-films. In block 330, a layer of passivation is applied over the previously applied layers on the substrate. In block 332, using the via mask, the passivation layer is patterned and etched to create a second set of contact regions in the passivation layer to the third conductive layer. Preferably the protective passivation layer is made up of a layer of silicon nitride and a layer of silicon carbide. In block 334, a protective cavitation layer is applied, preferably tantalum, tungsten, or molybdenum. In block 336, the cavitation layer is patterned with the cavitation mask and etched. In block 338, a fourth conductive layer, preferably gold, deposited or sputtered. The fourth conductive layer is patterned with the metal2 mask in block 340 and etched to create conductive traces. The fourth conductive layer traces are used to make contact with the third conductive layer through the second set of contact regions

in the passivation layer. External signals to operate the printhead make contact to the fourth conductive layer. In step 342, an orifice layer is applied over the surface of the previously applied stack of thin-film layers on the substrate. The orifice layer is made of one or more layers. One option is to provide a protective barrier layer to define fluid wells (fluid receiving cavities) coupled to the ejection elements, and then applying an orifice plate with nozzles defined therein over the fluid wells for directing any ejected fluid from the printhead. Another option is to apply a photolithographic polymer or epoxy material that can be exposed and developed to form the fluid well and nozzles. The polymer or epoxy material can be made of one or more layers.

A2 end

Please replace the paragraph beginning on page 9, line 15 with the following:

Fig. 6 is an exemplary schematic illustrating an electrical interface between a recording device and an integrated circuit that combines a transistor 130 with an ejection element 120. In this example, no substrate contact to ground potential is made. The bulk of transistor 130 is shown as having an inherent diode 13 between the bulk and the source 118 connections. In this example, the drain 116 of transistor 130 is coupled to an ejection element 120, a heater resistor. The heater resistor is further connected to a primitive driveline 46. A primitive is a grouping of ejection elements, such as a column of one color in printhead. Thus, the primitive signal interface 46, the gate 114 of the transistor 130 and the source 118 of the transistor 130 form external interface ports (such as contacts 214 in Fig. 9) that a recording device can control. The recording device 240 (see Fig. 10) includes a primitive select circuit 58 that controls power 56 via a switch 60 to preferably a group of ejection elements (a primitive) on the integrated circuit 200 (see Fig. 8). The recording device 240 also includes an address select circuit 66 that interfaces to a driver 62 that selects an individual ejection element within a primitive.

A3

In the Claims:

1. (Amended) An integrated circuit for a printhead, comprising:

a substrate;

a set of transistors formed in the substrate wherein the gate of each of the set of transistors forms at least one closed loop; and

an ejection element coupled to at least one of the set of transistors wherein the ejection element is disposed over the substrate without an intervening field oxide layer.

5. (Amended) The integrated circuit of claim 1 wherein each of the set of transistors has a bulk that is not directly connected to the substrate.

6. (Amended) The integrated circuit of claim 1 wherein the set of transistors is formed without an active mask definition.

7. (Amended) The integrated circuit of claim 1 wherein the set of transistors has a gate oxide formed with a layer of silicon dioxide and a layer of silicon nitride.

21. (Amended) A printhead having a set of transistors integrated thereon, the printhead comprising:

a substrate;

each transistor positioned on the substrate, the transistors comprising a source region, a drain region, and a gate positioned between the source region and the drain region, the gate forming a closed loop and comprising,

a layer of silicon dioxide not of field oxide disposed over the substrate, and

a layer of polycrystalline silicon directly on the layer of silicon dioxide;

a layer of dielectric material covering the substrate having a plurality of openings there through, the openings providing access the source region, the drain region, and the gate of the transistor;

a layer of electrically resistive material positioned on the layer of dielectric material and in direct electrical contact with the source region, the drain region, and the gate through the openings;

a layer of conductive material affixed to a portion of the layer of electrically resistive material in order to form a multi-layer structure , the layer of electrically resistive material having at least one uncovered section capable of functioning as an ejection element, the layer of electrically resistive material being covered with the layer of conductive material at the source region, the drain region and the gate of the transistor;

a portion of protective material positioned on the ejection element; and

an orifice layer having at least one nozzle, the orifice layer secured to the portion of protective material having a section thereof removed directly beneath the nozzle in order to form a fluid well in order to impart energy from the ejection element.